WHAT IS CLAIMED IS:

1. A method of manufacturing a pressure sensor having a boss comprising:

growing a first oxide layer on a bottom of a wafer, the wafer comprising a silicon-on-insulator structure having an insulator layer between a first silicon layer and a second silicon layer, a surface of the second silicon layer forming the bottom of the wafer;

selectively thinning at least one area of the first oxide layer such that a first thin-oxide area is formed;

removing the oxide layer from a first portion the first thin-oxide area such that a second thin-oxide area and a first exposed silicon area are formed; and

etching the bottom of the wafer such that the second silicon layer is removed above the first exposed silicon area and the second silicon layer is thinned above the second thin-oxide area, such that the boss is formed,

wherein the etching is a deep reactive ion etching, and

wherein the removal of the second silicon layer above the first exposed silicon area creates a sidewall, the sidewall substantially orthogonal to the bottom of the wafer.

2. The method of claim 1 further comprising:

non-selectively etching the pressure sensor.

3. The method of claim 2 wherein the non-selective etch is a KOH etch.

4. A pressure sensor comprising:

a horizontal diaphragm having a top and a bottom;

a silicon sidewall formed using MEMS mirco-machining and extending from the bottom of the diaphragm, the sidewall having an interior side forming a backside cavity, the backside cavity having a backside opening, the interior side substantially vertical; and

a boss attached to the bottom of the diaphragm, the boss separate from the sidewall.

5. The pressure sensor of claim 4 wherein the silicon sidewall is formed using deep reactive ion etch.

6. A method of manufacturing a pressure sensor comprising:

growing a first oxide layer on a bottom of a wafer, the wafer comprising a silicon-on-insulator structure including an insulator layer between a first silicon layer and a second silicon layer, a surface of the second silicon layer forming the bottom of the wafer;

selectively removing the first oxide layer such that a first no-oxide area is formed; and

etching the bottom of the wafer such that the second silicon layer is removed above the first no-oxide area,

wherein the etching is a deep reactive ion etching,

the first no-oxide area is non-rectangular, and

the removal of the second silicon layer above the first no-oxide area creates a sidewall, the sidewall substantially orthogonal to the bottom of the wafer.

7. The method of claim 6 wherein the first no-oxide area is shaped as a rounded rectangle.

8. The method of claim 6 wherein the first no-oxide area is shaped as a castle.

9. A pressure sensor comprising:

a diaphragm and a sidewall, the sidewall having an interior side defining a backside opening, the sidewall extending from the diaphragm to the backside opening,

wherein the interior side of the sidewall is formed using a deep reactive ion etch and is substantially orthogonal to the diaphragm, and

wherein the backside opening is non-rectangular.

10. The pressure sensor of claim 9 wherein the backside opening forms a rounded square.

11. The method of claim 9 wherein the backside opening is shaped as a castle.

12. A method of manufacturing a pressure sensor comprising:

growing a first oxide layer on a bottom of a wafer, the wafer comprising a silicon-on-insulator structure having a buried insulator layer between a first silicon layer and a second silicon layer, a surface of the second silicon layer forming the bottom of the wafer;

selectively removing the first oxide layer such that a first no-oxide area is formed;

etching the bottom of the wafer such that the second silicon layer is removed between the first no-oxide area and the buried insulator layer, such that an exposed portion of the buried insulator layer is formed; and

adjusting a sensitivity of the pressure sensor by thinning the exposed portion of the buried insulator layer,

wherein the etching is a deep reactive ion etching, and

wherein the removal of the second silicon layer above the first no-oxide area creates a sidewall, the sidewall substantially orthogonal to the bottom of the wafer.

13. The method of claim 12 further comprising:

further adjusting the sensitivity of the pressure sensor by removing the exposed portion the buried insulator layer such that an exposed portion of the first silicon layer is formed.

14. The method of claim 13 further comprising:

thinning the exposed portion of the first silicon layer by etching, wherein the etch is a deep reactive ion etch.

15. An absolute pressure sensor comprising:

a diaphragm having a top and a bottom;

a sidewall extending from the bottom of the diaphragm, the sidewall having an interior side forming a backside cavity having a backside opening, the interior side substantially orthogonal to the diaphragm; and

a block covering the backside opening such that a hermetic seal is formed.

16. The absolute pressure sensor of claim 15 wherein the block is silicon.

17. The absolute pressure sensor of claim 15 wherein the block is glass.

18. The absolute pressure sensor of claim 15 wherein the glass block is covered with metal over the backside opening.

19. A method of manufacturing a pressure sensor comprising:

growing a first oxide layer on a bottom of a first wafer, the first wafer comprising a silicon-on-insulator structure including an insulator layer between a first silicon layer and a second silicon layer, a surface of the second silicon layer forming the bottom of the first wafer;

selectively removing the first oxide layer such that a first exposed silicon area is formed;

etching the bottom of the wafer such that the second silicon layer is removed above the first exposed silicon area and a backside cavity having a backside opening is formed;

attaching a second wafer to the bottom of the first wafer such that the backside opening is covered such that a hermetic seal is formed; and

etching through the second wafer, such that an opening to the backside cavity is formed,

wherein the etching is a deep reactive ion etching, and

the removal of the second silicon layer above the first exposed silicon area creates a sidewall, the sidewall substantially orthogonal to the bottom of the first wafer.

20. A silicon wafer comprising:

a plurality of pressure sensors, each pressure sensor comprising:

a diaphragm having a top and a bottom; and

a sidewall extending from the bottom of the diaphragm, the sidewall having an interior side formed using a deep reactive ion etch and forming a backside cavity having a backside opening, the interior side substantially orthogonal to the diaphragm,

wherein the plurality of pressure sensors includes approximately at least twenty-thousand pressure sensors,

and wherein the silicon wafer is a 150mm (6 inch) wafer.

21. A pressure sensor apparatus comprising:

exactly one pressure sensor in a housing, the exactly one pressure sensor comprising:

a diaphragm having a top and a bottom; and

a sidewall extending from the bottom of the diaphragm, the sidewall having an interior side formed using a deep reactive ion etch and forming a backside cavity having a backside opening, the interior side substantially orthogonal to the diaphragm,

wherein the diaphragm is less than 350 microns in length, and

the diaphragm accounts for more than 10 percent of an area of the exactly one pressure sensor.

22. A pressure sensor comprising:

a diaphragm having a top and a bottom;

a sidewall extending from the bottom of the diaphragm, the sidewall having an interior side forming a backside cavity having a backside opening, the interior side substantially orthogonal to the diaphragm; and

a cap attached to the top of the diaphragm,

wherein the cap and diaphragm form a reference cavity.

23. The pressure sensor of claim 22 further comprising:

a first electrode attached to the top of the diaphragm; and

a second electrode attached to an underside of the cap,

wherein the first electrode and the second electrode form a capacitor.

24. The pressure sensor of claim 22 further comprising a plurality of resistors in the top of the diaphragm, wherein the plurality of resistors form a piezoresistive sensing circuit.